CLAIMS

1. An integrated circuit comprising:

a functional block of active circuitry formed within a die and configured to perform a function;

a passivation layer overlying a portion of a top surface of the die; and

a test pad structure for receiving test probes substantially disposed within a center region of the die, wherein the test pad structure includes a first portion not overlying the passivation layer that directly accesses the functional block and a second portion overlying the passivation layer configured for being probed during a testing of the functional block.

2. The integrated circuit of claim 1, further comprising

a plurality of bond pads along a periphery of the die; and

a via formed through the passivation layer for the first portion of the test pad structure. .

3. The integrated circuit of claim 2, wherein the bond pads are configured for at least two sets of signals, a first set of signals disposed for use only with metal layer pads on the periphery region, and a second set of signals disposed for use with both metal layer pads on the periphery region and the test pad structure, the second set of signals being sufficient to perform a test of the functional block.

4. The integrated circuit of claim 2, wherein the via includes multiple vias, the multiple vias configured per an electrical requirement of the test pad structure.

5. The integrated circuit of claim 2, wherein the test pad structure further includes an aluminum (Al) cap with a barrier layer disposed between the aluminum cap and the underlying passivation layer and functional block.

6. The integrated circuit of claim 2, wherein the test pad structure comprises a plurality of test pads each having a top surface area and the plurality of bond pads each having a top surface substantially smaller than the top surface area of the test pads.

7. The integrated circuit of claim 6 further comprising built-in self-test (BIST)circuitry and wherein the number of test pads sufficient for testing the functional block in conjunction with the BIST circuitry is not greater than 16.

8. The integrated circuit of claim 6, wherein the number of test pads is a function of a desired testing of the functional block.

9. The integrated circuit of claim 6, wherein the test pads are large size on the order of 100μm x 200μm and of coarse pitch on the order of between 200 to 250 μm.

10. The integrated circuit of claim 6, wherein the test pads are aligned within the center region for probing, wherein the probing includes one selected from the group consisting of cantilevered probing and vertical probing.

11. The integrated circuit of claim 10, further wherein the test pads are aligned in a single row.

12. The integrated circuit of claim 1, wherein the test pad structure includes at least one test pad configured for use with a signal solely for testing of the functional block.

13. The integrated circuit of claim 12, wherein the testing of the functional block is configured according to one selected from the group consisting of a built in self test (BIST), and a failure analysis test.

14. The integrated circuit of claim 13, further wherein the functional block and the test pad include a design for test (DFT) design of hardware and software integrated onto the integrated circuit.

15. The integrated circuit of claim 13, wherein the built in self test (BIST) enables use of a minimum required number of test pads for testing of the functional block.

16. The integrated circuit of claim 12, wherein the signal solely for testing of the functional block is not otherwise required at a metal layer pad on a periphery region of the die.

17. The integrated circuit of claim 1, wherein the test pad structure is not associated with a next-level interconnection.

18. The integrated circuit of claim 1, wherein the center region represents a core area of the die and excludes an area of I/O cells and metal layer pads on a periphery region of the die.

19. The integrated circuit of claim 1, wherein the functional block includes a memory of a system on chip (SOC).

20. The integrated circuit of claim 19, wherein the memory includes one selected from the group consisting of Flash, DRAM, SRAM, and ROM memory.

21. The integrated circuit of claim 20, further wherein the memory includes Flash memory on the order of 2 megabytes.

22. The integrated circuit of claim 1, wherein the functional block includes a logic of a system on chip (SOC).

23. The integrated circuit of claim 1, wherein the functional block includes multiple die functionalities of multiple functional blocks.

24. The integrated circuit of claim 1, wherein the functional block includes a portion of a final metal layer.

25. The integrated circuit of claim 24, wherein the final metal layer is one selected from the group consisting of copper and aluminum.

26. An integrated circuit comprising:

a functional block of circuitry formed within a die and configured to perform a function;

a passivation layer overlying a portion of a top surface of the die; and

a plurality of bond pads disposed on a periphery region of the die configured for a first set of functions and a second set of functions, wherein the first set of functions is exclusively for the bond pads; and

a plurality of test pads overlying a portion of the passivation layer and disposed within a center region of the die, wherein the plurality of test pads are for the second set of functions and wherein the second set of functions is for testing the functional block.

27. The integrated circuit of claim 26, wherein each of the plurality bond pads has a top surface area and each of the plurality of test pads has a top surface area that is at least twice that of each of the plurality of bond pads.

28. The integrated circuit of claim 26, wherein each of the plurality bond pads has a top surface area and each of the plurality of test pads has a top surface area at least about four times that of each of the plurality of bond pads.

29. The integrated circuit of claim 26, wherein the plurality of test pads are sufficient for testing the functional block.

30. The integrated circuit of claim 26, wherein each of the test pads is directly connected to the functional block through vias in the passivation layer.

31. The integrated circuit of claim 26, wherein each of the test pads is completely surrounded by the passivation layer.

32. A test apparatus for testing the integrated circuit of claim 26, comprising:

a tester for testing a functional block of the integrated circuit; and

a probe card coupled to the tester and having probe contacts,

wherein the probe contacts are configured for contacting the test pad structure of the integrated circuit during a test of the functional block by the tester.

33. A method for testing the integrated circuit of claim 26, comprising:

providing a tester for testing a functional block of the integrated circuit; and

supplying a probe card coupled to the tester and having probe contacts, wherein the probe contacts are configured for contacting the test pad structure of the integrated circuit during a test of the functional block by the tester.

34. The method of claim 33, wherein the probe contacts are further configured for contacting test pad structures of a plurality of integrated circuits on a wafer simultaneously for parallel testing, and wherein the tester is further for testing a functional block of the plurality of integrated circuits.

35. The method of claim 34, wherein the probe contacts are configured for contacting the test pad structures of at least sixteen integrated circuit die simultaneously.

36. The method of claim 35, wherein the probe contacts include cantilever probe contacts.

37. A method of making an integrated circuit comprising:

forming a functional block of active circuitry within a die, the functional block of active circuitry configured to perform a function;

forming a passivation layer overlying a portion of a top surface of the die; and

forming a test pad structure substantially overlying a portion of the passivation layer and disposed within a center region of the die, wherein forming the test pad structure includes forming a first portion of the test pad structure that directly accesses the functional block and forming another portion of the test pad structure for being probed during a testing of the functional block.

38. The method of claim 37, further comprising:

forming metal layer pads disposed on a periphery region of the die, wherein the metal layer pads are configured for at least two sets of signals, a first set of signals disposed for use only with metal layer pads on the periphery region, and a second set of signals disposed for use with both metal layer pads on the periphery region and the test pad structure, the second set of signals being sufficient to perform a test of the functional block.